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Bipolar Active Inductor Realizability Limits, Distortion, and Bias Considerations

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***Abstract*-Active inductors for MMICs offer an interesting alternative to passive implementations when the rf currents are below the threshold levels needed to maintain low distortion. This paper examines the limits of realizability for a MMIC inductor circuit that utilizes two bipolar junction transistors in a common collector-common emitter configuration to gyrate the base-emitter capacitance of the common emitter stage to form a synthetic inductor. The inductance range, Q-factor, distortion, dc bias points, and dc power consumption for the circuit are considered.**

Governing equations and graphs describing circuit performance are presented. The results show that the goals of higher Q, lower distortion, and good DC power utilization are not conflicting in terms of the biasing of the transistors.

1. INTRODUCTION

Active inductors are an alternative to using passive, lumped-element inductors in monolithic microwave integrated circuits (MMICs). They require less die area, have higher usable frequencies, and have the potential for higher Q's than a spiral inductor of equivalent inductance. Because the inductor is synthesized with active devices, they have two drawbacks that their passive counterparts do not, i.e., their nonlinear effects become significant at much lower signal levels and they consume dc power.

Recent circuits have been described for using field effect transistors (FET) as the active devices [1,2,3] as well as general architectures for floating immittances [4]. The FET circuits utilize resistive feedback. When considering similar circuits using bipolar devices, the input immitance often consists of a heavily damped parallel R-C circuit and the resulting inductor value varies with frequency and the circuit often turns out to have negative values for the real part of the impedance.

This work extends the previous work done by Campbell [5] and Campbell and Weber [6,7] and uses that particular circuit realization. Further analysis of Campbell's realization is performed to show that the equivalent series resistance of the resulting active inductor has both upper and lower bounds and is a function of the inductance value. This directly affects the Q-factor that can be attained. Bias considerations to minimize power dissipation without compromising the circuit's performance are discussed. Ultimately, this analysis demonstrates that the mutual goals of maximum Q, low distortion, and good utilization of dc power are not conflicting in regards to the bias considerations of the two transistors.

The circuit used to synthesize the inductor is shown in figure 1. It consists of two bipolar junction transistors (BJTs), one a common emitter and the other a common collector in a gyrator configuration to synthesize an active inductor. This circuit also employs two series-connected parallel resistor-capacitor networks in feedback to compensate for the base-emitter poles of the two transistors and provide a relatively constant inductance over a wide frequency range.

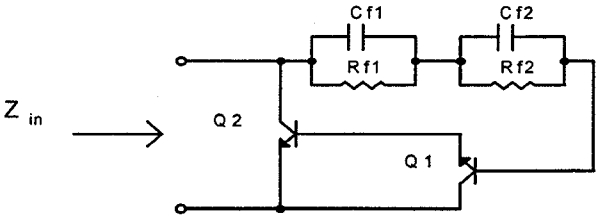

Figure 1 - Active inductor circuit (from Campbell [5]).

2. REALIZABILITY LIMITATIONS

The realization of an active two terminal network whose input impedance is an inductance in series with a resistance, over a very broad frequency range, is covered extensively by Campbell [5]. Campbell shows that, in order for the circuit to realize an inductance in series with a resistance, i.e., $Z_{in}(\omega) = R_{in}(\omega) + j\omega L_{in}(\omega)$, the driving point impedance of the feedback network must be

$$Z_f(s) = \frac{K(s+\sigma_z)}{\left(s+\frac{1}{R_{\pi 1}C_{\pi 1}}\right)\left(s+\frac{1}{R_{\pi 2}C_{\pi 2}}\right)} \quad (1)$$

where

$$K = \frac{g_{m2}}{C_{\pi 1}C_{\pi 2}}\left(L_{in}(\omega)g_{m1} + C_{\pi 1}R_{in}(\omega) - \frac{L_{in}(\omega)C_{\pi 1}}{R_{\pi 2}C_{\pi 2}}\right) \quad (2)$$

$$\sigma_z = \frac{R_{in}(\omega)\left(g_{m1}+\frac{1}{R_{\pi 1}}\right) - \frac{L_{in}(\omega)}{R_{\pi 1}R_{\pi 2}C_{\pi 2}} - \frac{g_{m1}}{g_{m2}}}{L_{in}(\omega)\left(g_{m1}-\frac{C_{\pi 1}}{R_{\pi 2}C_{\pi 2}}\right) + R_{in}(\omega)C_{\pi 1}} \quad (3)$$

Since the inductance and resistance have a slight frequency dependence, they are shown as explicit functions of frequency.

The key to realizing this network comes from the theory of driving point impedances. In general, a real

rational function can be the driving point impedance of a one port network if and only if all the poles and zeros are 1) simple, 2) lie on the negative real axis, and 3) alternate with each other[8]. The first critical frequency must be a pole. For the function in (1), this implies that the zero, σ_z, must lie between the two poles. Thus, there are two possible solutions, either

$$\frac{1}{R_{\pi 1} C_{\pi 1}} > \sigma_z > \frac{1}{R_{\pi 2} C_{\pi 2}} \tag{4}$$

or

$$\frac{1}{R_{\pi 2} C_{\pi 2}} > \sigma_z > \frac{1}{R_{\pi 1} C_{\pi 1}} \tag{5}$$

depending on which pole occurs first.

The function in (1) can be realized in the form of two parallel RC networks connected in series as was shown in figure 1. The values of these feedback elements are given by

$$R_{f1} = R_{\pi 1} C_{\pi 1} A \tag{6}$$

$$C_{f1} = \frac{1}{A} \tag{7}$$

$$C_{f2} = \frac{1}{B} \tag{8}$$

$$R_{f2} = R_{\pi 2} C_{\pi 2} B \tag{9}$$

with

$$A = \frac{K\left(\sigma_z - \frac{1}{R_{\pi 1} C_{\pi 1}}\right)}{\frac{1}{R_{\pi 2} C_{\pi 2}} - \frac{1}{R_{\pi 1} C_{\pi 1}}} \tag{10}$$

$$B = \frac{K\left(\sigma_z - \frac{1}{R_{\pi 2} C_{\pi 2}}\right)}{\frac{1}{R_{\pi 1} C_{\pi 1}} - \frac{1}{R_{\pi 2} C_{\pi 2}}} \tag{11}$$

Depending on whether $1/R_{\pi 1}C_{\pi 1}$ is greater or less than $1/R_{\pi 2}C_{\pi 2}$, either (4) or (5) applies in a particular realization. It will be shown that (5) applies when distortion and DC power utilization are considered later.

As is now shown, these requirements result in upper and lower bounds on the equivalent series resistance of the inductor once the desired inductance value and the bias points for Q1 and Q2 are selected

To begin, the limit where σ_z equals $1/R_{\pi 1}C_{\pi 1}$ is determined. Setting the right side of (3) equal to $1/R_{\pi 1}C_{\pi 1}$ and solving for $R_{in}(\omega)$ gives

$$R_{in(1)}(\omega) = L_{in}(\omega)\frac{1}{R_{\pi 1} C_{\pi 1}} + \frac{1}{g_{m2}} \tag{12}$$

where the subscript "(1)" denotes that this is for the case of σ_z equal to $1/R_{\pi 1}C_{\pi 1}$.

In a similar manner, setting the right side of (3) equal to $1/R_{\pi 2}C_{\pi 2}$ and solving for $R_{in}(\omega)$ gives

$$R_{in(2)}(\omega) = L_{in}(\omega)\frac{1}{R_{\pi 2} C_{\pi 2}} + \frac{1}{g_{m2}\left(1 + \frac{R_{\pi 2} C_{\pi 2} - R_{\pi 1} C_{\pi 1}}{g_{m1} R_{\pi 1} R_{\pi 2} C_{\pi 2}}\right)} \tag{13}$$

where the subscript "(2)" denotes that this is for the case of σ_z equal to $1/R_{\pi 2}C_{\pi 2}$.

The Q-factor of any inductor is defined as the ratio of energy stored, to energy lost, per cycle. For the active inductor, the Q-factor will be approximated by the ratio of the inductive reactance to the series resistance and will exhibit a frequency dependence:

$$Q(\omega) = \frac{\omega L_{in}(\omega)}{R_{in}(\omega)} \tag{14}$$

Since $R_{in}(\omega)$ is bounded, $Q(\omega)$ must also be bounded. Substituting (14) into (12) and (13) gives the following expressions for the two bounds on $Q(\omega)$.

$$Q_{(1)}(\omega) = \frac{\omega}{\frac{1}{R_{\pi 1} C_{\pi 1}} + \frac{1}{L_{in}(\omega) g_{m2}}} \tag{15}$$

$$Q_{(2)}(\omega) = \frac{\omega}{\frac{1}{R_{\pi 2} C_{\pi 2}} + \frac{1}{L_{in}(\omega) g_{m2}\left(1 + \frac{R_{\pi 2} C_{\pi 2} - R_{\pi 1} C_{\pi 1}}{g_{m1} R_{\pi 1} R_{\pi 2} C_{\pi 2}}\right)}} \tag{16}$$

For the case of (5) it is apparent that (12) characterizes the minimum bound on R_{in} and (15) the maximum bound on Q. It is also apparent that when L=0, R_{in} is positive and non-zero. Thus, a lossless inductor cannot be realized with this circuit.

3. TRANSISTOR BIASING ISSUES

For the following analysis, it is assumed that the two transistors, Q1 and Q2, are identical. This means that the same values of both collector current and collector-emitter voltage cannot be used for both transistors because, if the base-emitter poles are identical, the conditions for (4) or (5) are violated. If the same collector-emitter voltage is used for both transistors, they must be biased to different collector currents. This leads naturally to the question of which transistor should have the greater collector current, Q1 or Q2? To answer this, we begin by assuming that the transistors always remain in the active region where $V_{BE} \gg kT/q$ and $V_{BC} \leq 0$.

Following Antognetti and Massobrio [9], the pertinent elements of the hybrid-pi model can be shown to be

$$R_{\pi} = \frac{\beta_F}{\frac{q}{kT} I_C} \tag{17}$$

$$C_\pi = \frac{q}{kT}\tau_F I_C + C_{JE}(V_{BE}) \quad (18)$$

Since V_{BE} does not change much, $C_{JE}(V_{BE})$ can also be treated as a constant C_{JE}.

What can be seen from these equations is that all the hybrid-pi parameters are determined by the collector current I_C. As I_C increases, g_m increases, C_π increases, and R_π decreases. Multiplying both sides of (17) by (18) and treating $C_{JE}(V_{BE})$ as a constant equal to C_{JE} gives

$$R_\pi C_\pi = \beta_F \tau_F + \frac{\beta_F C_{JE}}{\frac{q}{kT} I_C} \quad (19)$$

Thus, as I_C increases, $R_\pi C_\pi$ decreases and the frequency location of the base-emitter pole $1/R_\pi C_\pi$ increases.

For the case where Q2 is biased with more collector current than Q1, the lower bound for $R_{in}(\omega)$ is given by (12) and the upper bound for $Q(\omega)$ is given by (15). The expressions for the various hybrid-pi parameters can be substituted into (12) to give

$$R_{in(l)}(\omega) = L_{in}(\omega)\frac{1}{\beta_F \tau_F + \frac{\beta_F C_{JE}}{\frac{q}{kT} I_{C1}}} + \frac{1}{\frac{q}{kT} I_{C2}} \quad (20)$$

This equations shows that $R_{in}(\omega)$ is decreased by increasing I_{C2} and/or by decreasing I_{C1}. The only limits to minimizing $R_{in}(\omega)$, and therefore maximizing $Q(\omega)$ for this condition, are the limits imposed by the actual transistors used. The collector current of Q2 can be increased up to its maximum allowable value. The collector current of Q1 need only to be large enough to keep Q1 active while driving the base of Q2.

4. DISTORTION IN THE ACTIVE INDUCTOR

There are several mechanisms that can cause this active inductor circuit to become nonlinear. From the theory presented earlier, the value of the inductance is determined by the value of the feedback elements and the hybrid-pi model components. It is practical and valid to assume that the feedback elements of the circuit are linear. When the transistors in the circuit are driven with a large signal, however, the small-signal assumption is no longer valid, i.e. the operating point varies because of the large signal swings. When this happens, the hybrid-pi model components are no longer constant, but vary with signal amplitude. The result is signal distortion induced by the non-linear model components.

A more pronounced distortion mechanism is caused by current limiting. The onset of this distortion is dramatic when the peak amplitude of the AC current through either transistor exceeds its dc bias current. Since Q1 is driving Q2, the magnitude of the AC current in Q1 is much less than in Q2. Thus, Q1 can be biased at a much lower DC current than Q2 without affecting distortion. This also results in lower power dissipation.

5. SIMULATION RESULTS

As an example, SPICE simulations were performed with the vendor-supplied Gummel-Poon model parameters for the NEC NE681 with Q1 biased at 8V and 3mA, and Q2 biased at 8V and 10mA. At these bias points, g_{m1} = 0.109 S, $R_{\pi 1}$ = 977 Ω, $C_{\pi 1}$ = 4.11 pF, $g_{\pi 2}$ = 0.342 S, $R_{\pi 2}$ = 373 Ω, and $C_{\pi 2}$ = 7.63 pF. Figure 2 is a plot of the upper and lower bounds given by (12) and (13). The shaded region shows the possible combinations of inductance and series resistance that may be synthesized by the circuit once the bias points are established. Values of resistance and inductance outside this region are not realizable. A plot of the region of realizability of Q at 500 MHz is shown in figure 3. Choosing an inductance value of 5nH with a series resistance of 4.4 Ω results in feedback elements of R_{f1} = 10.767 kΩ, C_{f1} = 0.373 pF, R_{f2} = 9.621 kΩ, and C_{f2} = 0.296 pF.

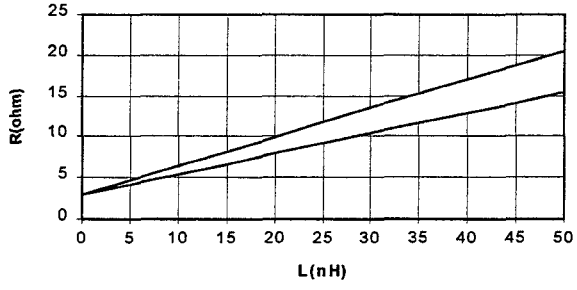

Figure 2 - Realizability region for Rin

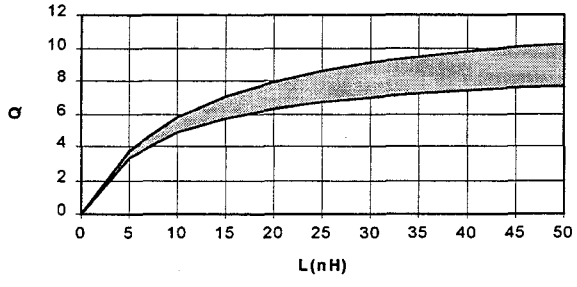

Figure 3 - Realizability region for Q

Results of small-signal SPICE simulations of the inductance and resistance values as a function of frequency are shown in figures 4. The results show

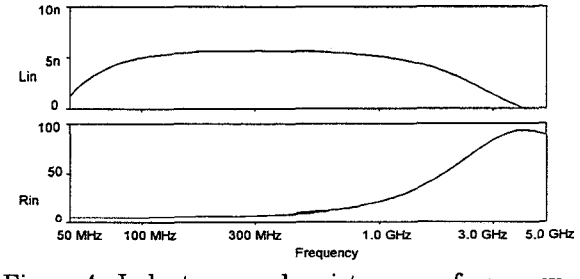

Figure 4 - Inductance and resistance vs. frequency

that the inductance and resistance are relatively constant in the frequency range of 100 MHz to 1 GHz. The inductance simulated is within 5% of the design value. The series resistance, however, is about twice as much as the design value. The roll-off at lower frequencies is due to the coupling capacitors used. The high frequency roll-off is caused by the circuit model. As the frequency increases, the simple three element hybrid-pi model looses validity and thus the theory used to develop the circuit is no longer applicable. This effect was described by Campbell [5].

The large-signal behavior of the active inductor circuit was studied in the time domain by using the transient analysis feature of SPICE. The .FOUR statement was used to produce a table of the magnitude and phase of the fundamental through ninth harmonic of the inductor terminal voltage when driven by a sinusoidal current. Figure 6 shows the results of the harmonic distortion analysis. The amplitudes of the second through seventh harmonics, normalized to the amplitude of the fundamental, are plotted as a function of the peak current into the active inductor. The second harmonic rises sharply when the peak inductor current approaches the 10 mA bias current of Q2. The total harmonic distortion is also given in the SPICE output file. As the peak inductor current increases to one-half of the bias current through Q2, the distortion rises to 7 percent and is 18 percent when the peak inductor current level equals the Q2 bias current.

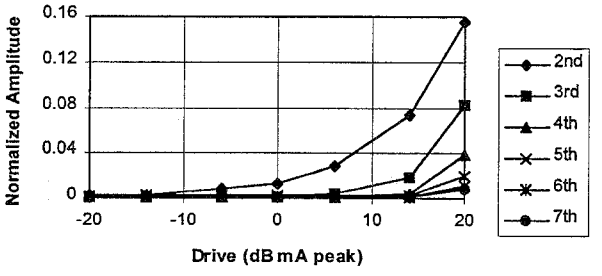

Figure 5 - Harmonic levels vs drive level

6. CONCLUSIONS

The previously published theory underlying the bipolar active inductor circuit used for this study was reviewed.

The region of realizable series resistance that is possible once a value for the inductance is selected was explored. Bias considerations to maximize the quality factor of the inductor were investigated. The bias condition where the collector current of Q2 is made as large as possible and for Q1 is made as small as possible results in the greatest limiting value for Q.

The level at which distortion occurs is primarily determined by the bias on Q2. Simulations were performed to demonstrate the performance of the active inductor. The results showed that, as the inductor current approaches the bias current of Q2, the distortion rises to 18 percent. The power dissipation of the circuit can be reduced by reducing the bias on Q1 without compromising the performance of the circuit. Thus, the bias considerations that serve to increase Q, reduce distortion, and increase the utilization of dc power are not conflicting. A more thorough discussion of this subject may be found in [10].

REFERENCES

1. Hara, S., Tokumitsu, T., Tanaka, T. and M. Aikawa, "Broad-Band Monolithic Microwave Active Inductor and its Application to Miniaturized Wide-Band Amplifiers," IEEE Transactions on Microwave Theory and Techniques, MTT-36, No. 12 (December 1988), pp. 1920-1924.

2. Hara, S., Tokumitsu, T. and M. Aikawa, "Lossless Broad-Band Monolithic Microwave Active Inductors," IEEE Transactions on Microwave Theory and Techniques, MTT-37, No. 12 (December 1989), pp. 1979-1984.

3. Zhang, G.F., Ripoll, C.S., and M.L.Villegas, "GaAs Monolithic Microwave Floating Active Inductor," Electronics Letters, 26th September 1991, Vol. 27, No. 20, pp. 1860-1862.

4. Hagashimura, M. and Y. Fukui, " Novel Method for Realizing Lossless Floating Immitance Using Current Conveyors," Electronics Letters, 7th May 1987, Vol. 23, No. 10, pp. 498-499.

5. Campbell, C.F., "Design and Performance of a Broadband Microwave Active Inductor Circuit with an Application to Amplifier Design," M.S. Thesis, Iowa State University, 1991.

6. Campbell, C.F. and R.J. Weber, "Design of a Broadband Microwave BJT Active Inductor Circuit," 34th Midwest Symposium on Circuits and Systems, held in Monterey, California, 1991, IEEE Circuits and Systems Society.

7. Campbell, C.F. and R.J. Weber, US Patent No. 5,256,991 - "Broadband Microwave Active Inductor Circuit," October 26, 1993.

8. Van Valkenburg, M.E., Network Analysis, Prentice Hall, pg 222, 1955.

9. Antognetti, P. and G. Massobrio, Semiconductor Device Modelling with SPICE, New York, McGraw-Hill, 1988.

10. Anderson, D.P., "Realizability Limits, Distortion, and Bias Considerations of a Bipolar Active Inductor," M.S. Thesis, Iowa State University, 1993.